Power Supply IC Series for TFT-LCD Panels

Automotive Panel Power Management IC

BD81842MUV-M

●General Description

The BD81842MUV-M is a power management IC for TFT-LCD panels which are used in car navigation, in-vehicle center panel, and instrument cluster. Incorporates high-power FET with low on resistance for large currents that employ high-power packages, thus driving large current loads while suppressing the generation of heat. A charge pump controller is incorporated as well, thus greatly reducing the number of application components. Also Gate Shading Function is included.

●Key Specifications

■ Input voltage range :	2.0V to 5.5V
■ AVDD Output voltage range :	6.0V to 18V
■ SRC Output voltage range :	12V to 34V
■ VCOM Output current :	200mA (Typ.)
■ Oscillator Frequency :	2.1MHz (Typ.)
■ Operating temperature range :	-40℃ to +105℃

●Special Characteristics

■ FB Regulation voltage :	±3% (Ta=-40～105℃)
■ Oscillator Frequency :	±10.5% (Ta=-40～105℃)

●Applications

TFT-LCD Panels which are used in car navigation, in-vehicle center panel, and instrument cluster.

●Features

- AEC-Q100 Qualified(Note 1)
- Boost DC/DC converter; 18 V / 2.5 A switch current.
- Switching frequency: 2.1 MHz
- Operational Amplifier (short current 200mA)
- Incorporates Positive / Negative Charge-pump Controllers.
- Gate Shading Function
- Protection circuits:
  - Under Voltage Lockout Protection Circuit
  - Thermal Shutdown Circuit (Latch Mode)
  - Over Current Protection Circuit (AVDD)
  - Timer Latch Mode Short Circuit Protection (AVDD SRC /VGL)
  - Over / Under Voltage Protection Circuit for Boost DC/DC Output
  - No SCP time included (185ms from UVLO-off)

(Note1: Grade 2)

●Package

	W(Typ.) x D(Typ.) x H(Max.)
VQFN24SV4040	4.0mm x 4.0mm x 1.0mm

●Typical Application Circuit (TOP VIEW)

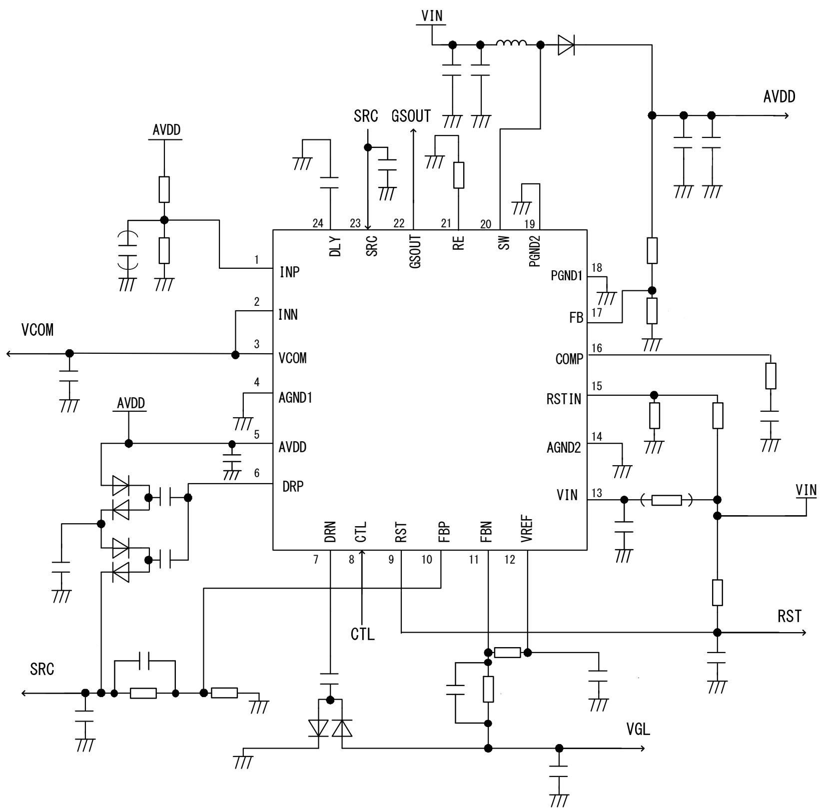


Figure 1. Application Circuit

○Product structure：Silicon monolithic integrated circuit ○This product is not designed for protection against radioactive rays

Contents

●Pin Configuration (TOP VIEW)

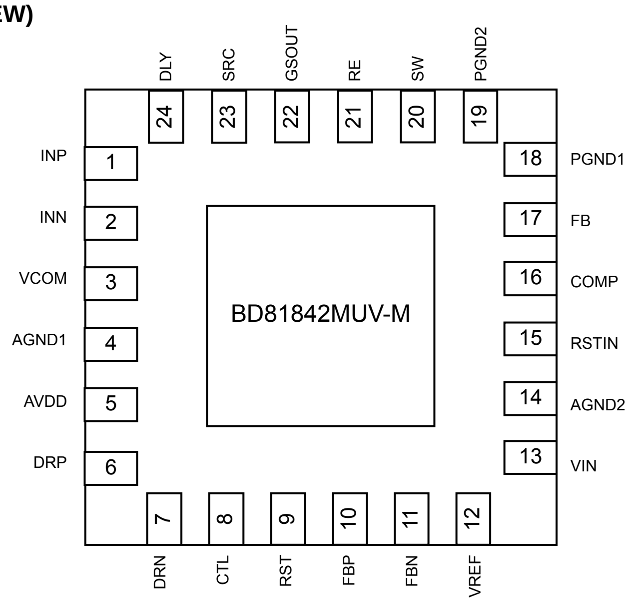


Figure 2. Pin Configuration

●Pin Descriptions

Pin No.	Pin Name	Function
1	INP	VCOM Amplifier input +
2	INN	VCOM Amplifier input -
3	VCOM	VCOM Amplifier output
4	AGND1	Ground
5	AVDD	Supply voltage input for VCOM, charge pump
6	DRP	Drive pin of the positive charge pump
7	DRN	Drive pin of the negative charge pump
8	CTL	High voltage switch control pin
9	RST	Open drain reset output
10	FBP	Positive charge pump feed back
11	FBN	Negative charge pump feed back
12	VREF	Internal Reference voltage output
13	VIN	Supply voltage input for PWM
14	AGND2	Ground
15	RSTIN	Reset comparator input
16	COMP	BOOST Error amplifier output
17	FB	BOOST Error amplifier input
18	PGND1	BOOST FET ground
19	PGND2	BOOST FET ground
20	SW	BOOST FET Drain
21	RE	Gate High voltage Fall set pin
22	GSOUT	Gate High voltage output set pin
23	SRC	Gate High voltage input set pin
24	DLY	GSOUT Delay Adjust pin

● **Block Diagram**

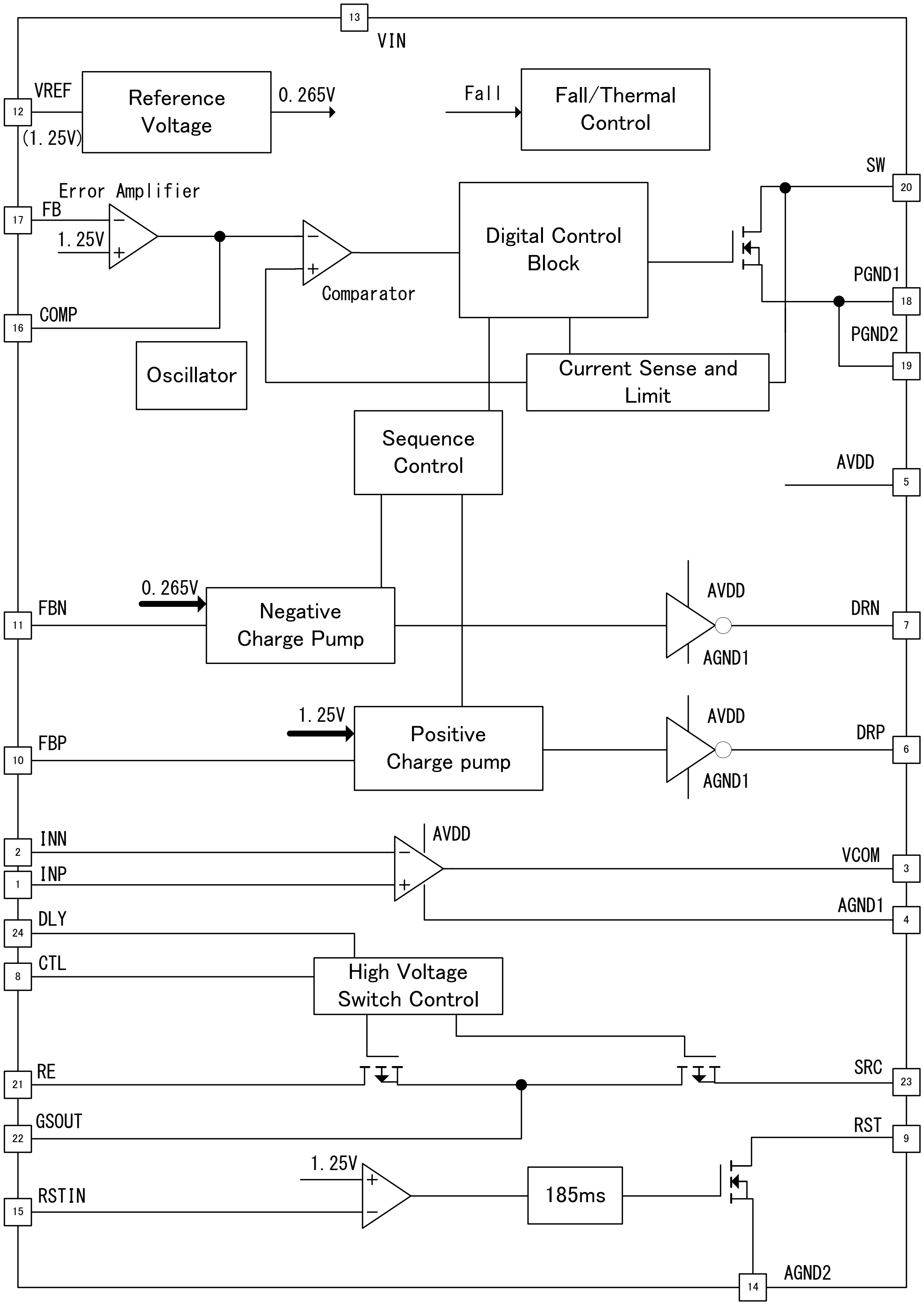


Figure 3. Block Diagram

●Main Block Function

・Boost Converter

A controller circuit for DC/DC boosting.
The switching duty is controlled so that the feedback voltage FB is set to 1.25 V (typ.).
A soft start operates at the time of starting.

・Positive Charge Pump

A controller circuit for the positive-side charge pump.
The switching amplitude is controlled so that the feedback voltage FBP will be set to 1.25 V (typ.).

・Negative Charge Pump

A controller circuit for the negative-side charge pump.
The switching amplitude is controlled so that the feedback voltage FBN will be set to 0.265 V (Typ.).

・Gate Shading Controller

A controller circuit for P-MOS FET Switch
The GSOUT switching synchronize with CTL input.
Please input voltage below VIN to CTL.
When VIN drops below UVLO threshold or RST=Low(=RSTIN<1.25V), GSOUT is pulled High(=SRC).

・VCOM

1-channel operational amplifier block.

・Reset

An open-drain output(RST) refer from RSTIN voltage(up to threshold voltage 1.25V).
RST keeps High(need a pull-up resistor connected to VIN) dulling to 185ms from start-up.

・VREF

A block that generates internal reference voltage of 1.25V (Typ.).
VREF is keep High when the thermal/short-current-protection shutdown circuit.

・TSD/UVLO/OVP/UVP

The thermal shutdown circuit is shut down at an IC internal temperature of 160℃.
The under-voltage lockout protection circuit shuts down the IC when the VIN is 1.85 V (Typ.) or below.
The over-voltage protection circuit when the AVDD is 20 V (Typ.) or over.
The under-voltage protection circuit when the AVDD is 1.3 V (Typ.) or under

・Start-up Controller

A control circuit for the starting sequence.
Controls to start in order of VIN →VGL →AVDD→SRC
(Please refer to Fig.27 of 16 page for details.)

●Absolute Maximum Ratings(Ta= 25℃)

PARAMETER	SYNBOL	LIMITS			Unit
		MIN	TYP	MAX	
Power Supply Voltage	VIN	-0.3	-	7	V
Output Pin	AVDD, SW, DRP, DRN, VCOM	-0.3	-	20	V
	SRC, GSOUT, RE	-0.3	-	36	V
	RST, COMP, VREF	-0.3	-	7	V
	SRC – GSOUT	-0.3	-	40	V
Input Pin	FB, FBP, FBN	-0.3	-	VIN+0.3	V
	INN, INP	-0.3	-	20	V
Function Pin Voltage	RSTIN, DLY, CTL	-0.3		VIN+0.3	V
Maximum Junction Temperature	Tjmax	-	-	150	℃
Operating Temperature Range	Topr	-40	-	105	℃
Storage Temperature Range	Tstg	-55	-	150	℃

●Thermal Resistance(Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 4)	2s2p(Note 5)	
VQFN24SV4040				
Junction to Ambient	θ_{JA}	150.6	37.9	℃/W
Junction to Top Characterization Parameter(Note 3)	Ψ_{JT}	20	9	℃/W

(Note 2)Based on JESD51-2A(Still-Air).
(Note 3)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4)Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 5)Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 6)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 6) This thermal via connects with the copper pattern of all layers.

●Recommended Operating Range

Parameter	Symbol	MIN	TYP	MAX	Unit
Power Supply Voltage	VIN	2.0	-	5.5	V
Output Pin	AVDD	6	-	18	V
	SRC	12	-	34	V

●**Electrical characteristics** (unless otherwise specified VIN = 3.3V, AVDD = 10V and Ta=25℃)

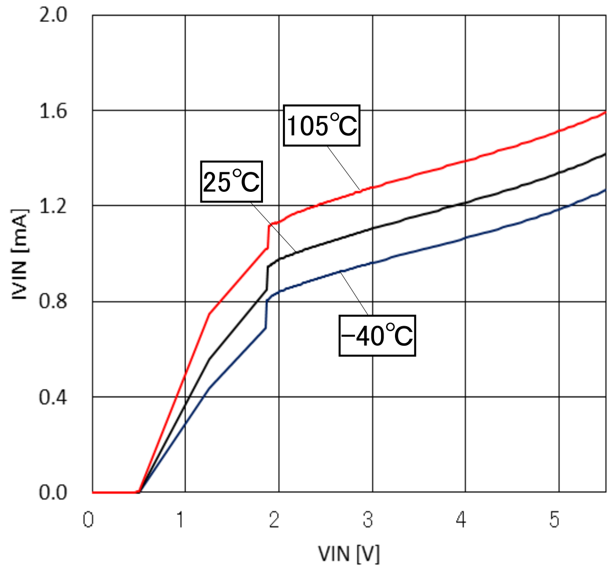
Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Condition
GENERAL						
Circuit Current	I_{VIN}	-	1.2	3	mA	No Switching Ta=-40～105℃
Under Voltage Lockout Threshold	V_{UVLO}	1.75	1.85	1.95	V	VIN rising Ta=-40～105℃
Internal Reference Output Voltage	VREF	1.225	1.25	1.275	V	No load Ta=25℃
		1.2125	1.25	1.2875	V	No load Ta=-40～105℃
Thermal Shutdown (rising)	TSD	-	160	-	℃	Junction Temp
Duration to Trigger Fault Condition	T_{SCP}	51	63	75	ms	FB , FBP or FBN below threshold
BOOST CONVERTER (AVDD)						
FB Regulation Voltage	V_{FB}	1.2375	1.25	1.2625	V	Ta=25℃
		1.2125	1.25	1.2875	V	Ta=-40～105℃
FB Fault Trip Level	V_{TL_FB}	0.9	1.0	1.1	V	FB falling
FB Input Bias Current	I_{FB}	-	0.1	2	μA	FB= 1.5V Ta=-40～105℃
SW Leakage Current	I_{SW_L}	-	0	10	μA	SW=20V Ta=-40～105℃
Maximum switching Duty Cycle	M_{DUTY}	85	90	95	%	FB= 1.0V
SW ON-Resistance	R_{SW}	-	200	250	mΩ	SW= 200mA
SW Current Limit	I_{SWLIM}	2.5	4.5	6.5	A	Ta=-40～105℃
Over Voltage Protection	V_{OVP}	18	20	22	V	AVDD rising
Under Voltage Protection	V_{UVP}	1	1.3	3	V	AVDD falling
BOOST Soft Start Time	T_{SS_FB}	12.5	15.5	18.5	ms	Ta=-40～105℃
Oscillator frequency	F_{SW}	1.9	2.1	2.3	MHz	Ta=25℃
		1.88	2.1	2.32	MHz	Ta=-40～105℃
RESET						
RST Output Low Voltage	V_{RST}	-	0.05	0.2	V	RST =1.2mA
RSTIN Threshold Voltage	V_{TH_L}	1.18	1.25	1.32	V	RSTIN rising Ta=-40～105℃
RSTIN Input Current	I_{RSTIN}	-	0	6	μA	RSTIN=0 to VIN-0.3 Ta=-40～105℃
RST Blanking Time	T_{NO_SCP}	165	185	205	ms	No SCP Zone Ta=-40～105℃
Operational Amp rifer						
Input Range	V_{RANGE}	0	-	AVDD	V	
Offset Voltage	V_{OS}	-	2	15	mV	INP= 5.0V
Input Current	I_{INP}	-	0	3	μA	INP= 5.0V Ta=-40～105℃
Output Swing Voltage (INP= 5.0V)	V_{OH}	-	5.03	5.06	V	VCOM = +50mA
	V_{OL}	4.94	4.97	-	V	VCOM = -50mA
Short Circuit Current	I_{SHT_VCOM}	-	200	400	mA	INP= 5.0V
Slew Rate	SR	10	40	250	V/us	

●**Electrical characteristics** (unless otherwise specified VIN = 3.3V, AVDD = 10V and Ta=25℃) (Continued)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Negative Charge pump driver (VGL)						
FBN Regulation Voltage	V_{FBN}	242	265	288	mV	Ta=25℃
		239	265	291	mV	Ta=-40～105℃
FBN Fault Trip Level	V_{TL_FBN}	400	450	500	mV	FBN rising
FBN Input Bias Current	I_{FBN}	-	0.1	15	µA	FBN= 0.1V Ta=-40～105℃
Oscillator frequency	F_{CPN}	425	525	625	kHz	Ta=-40～105℃
DRN Leakage Current	I_{DRN_L}	-	0	10	µA	FBN=1.0V Ta=-40～105℃
Positive Charge pump driver (SRC)						
FBP Regulation Voltage	V_{FBP}	1.2325	1.25	1.2675	V	Ta=25℃
		1.2125	1.25	1.2875	V	Ta=-40～105℃
FBP Fault Trip Level	V_{TL_FBP}	0.95	1.0	1.05	V	FBP falling
FBP Input Bias Current	I_{FBP}	-	0.1	15	µA	FBP= 1.5V Ta=-40～105℃
Oscillator frequency	F_{CPP}	425	525	625	kHz	Ta=-40～105℃
DRP Leakage Current	I_{DRP_L}	-	0	10	µA	FBP= 1.5V Ta=-40～105℃
Soft-Start Time	T_{SSP}	3.2	3.9	4.6	ms	Ta=-40～105℃
Gate Shading Function (GSOUT)						
DLY Source Current	I_{DLY}	3.5	5	6.5	µA	Ta=-40～105℃
DLY Threshold Voltage	V_{TL_DLY}	0.85	1.25	1.65	V	DLY falling Ta=-40～105℃
CTL Input Voltage High	V_{IN_H}	VIN ×0.65	-	VIN	V	Depend on VIN Ta=-40～105℃
CTL Input Voltage Low	V_{IN_L}	0	-	VIN ×0.25	V	Depend on VIN Ta=-40～105℃
CTL Input Bias Current	I_{CTL}	-	0	6	µA	RSTIN=0 to VIN-0.3 Ta=-40～105℃
Propagation delay time (Rising)	T_{GS_R}	-	100	200	ns	SRC= 25V
Propagation delay time (Falling)	T_{GS_F}	-	100	200	ns	SRC= 25V
SRC -GSOUT ON Resistance	R_{GS_H}	-	15	30	Ω	DLY = 1.5V
GSOUT-RE ON Resistance	R_{GS_M}	-	30	100	Ω	DLY = 1.5V
GSOUT-GND ON Resistance	R_{GS_L}	-	2.5	5.0	kΩ	DLY = 1.0V

○This product is not designed for protection against radio active rays.

●**Electrical characteristic curves (Reference data)**
(Unless otherwise specified VIN = 3.3V, AVDD = 10V and Ta=25℃)



Figuire 4. Circuit Current
(No switching)

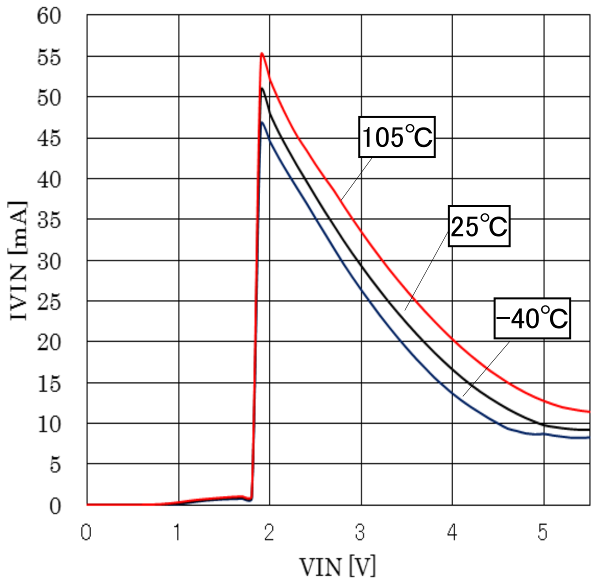


Figure 5. Circuit Current
(Switching)

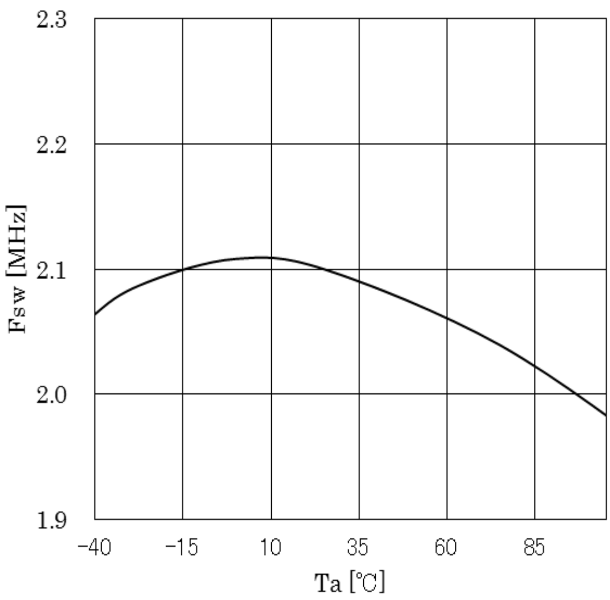


Figure 6. Dependent on
Temperature Frequency

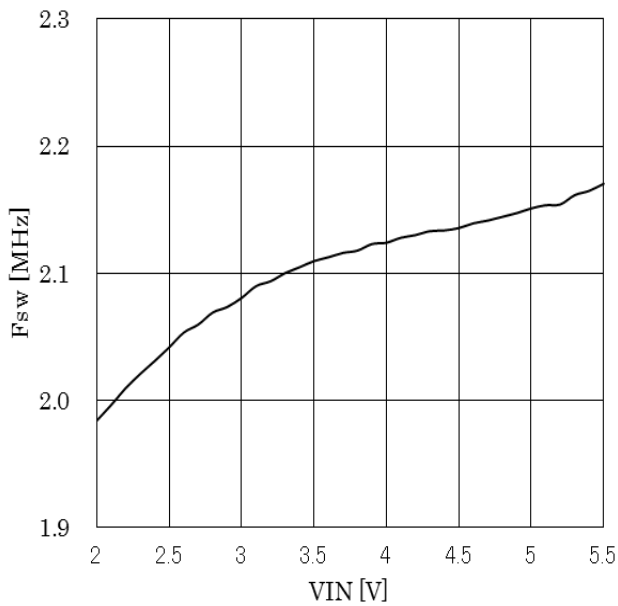


Figure 7. Dependent on Input
Voltage Frequency

● **Electrical characteristic curves (Reference data)**

(Unless otherwise specified VIN = 3.3V, AVDD = 10V and Ta=25℃)

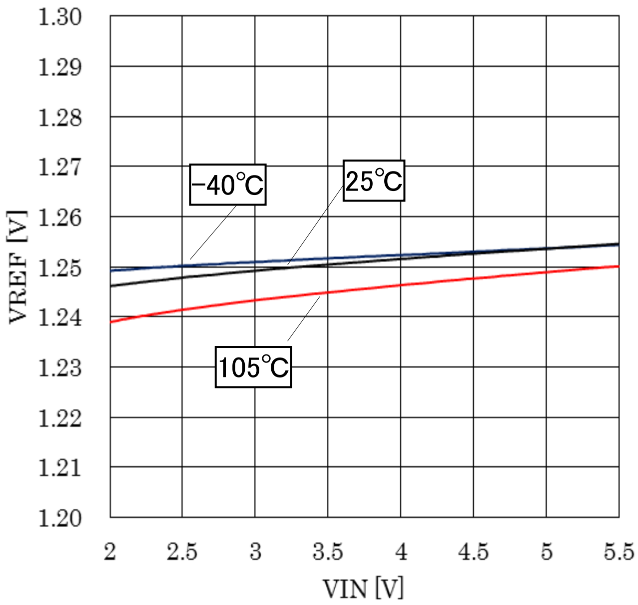


Figure 8. VREF Line Regulation

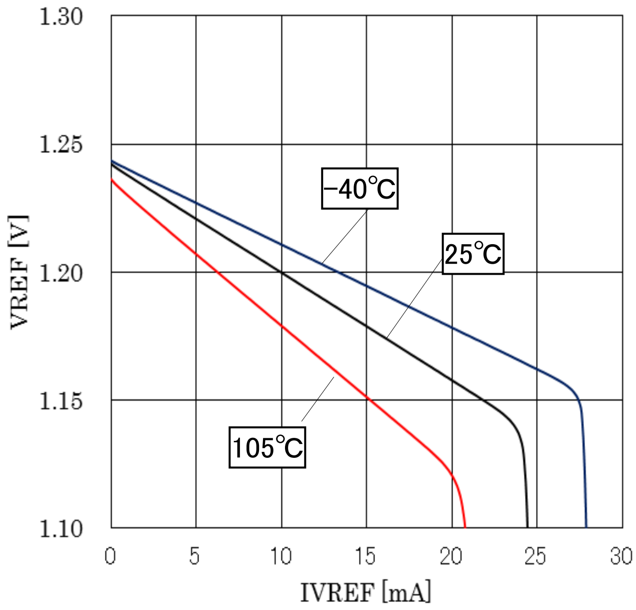


Figure 9. VREF Load Regulation

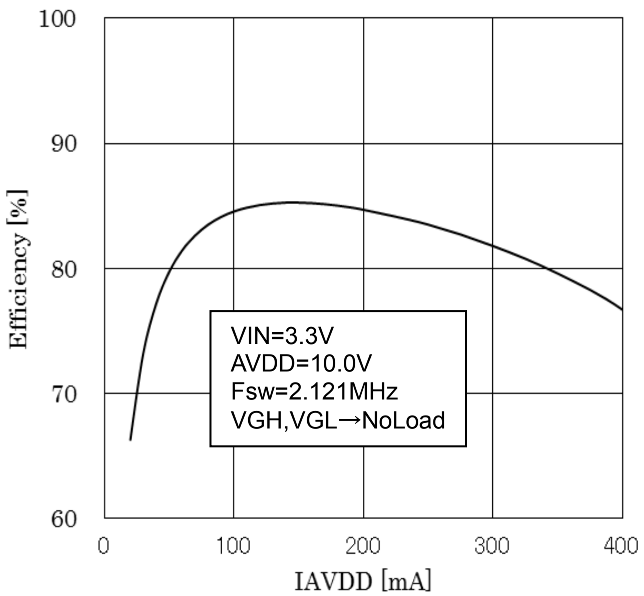


Figure 10. Boost Converter Efficiency

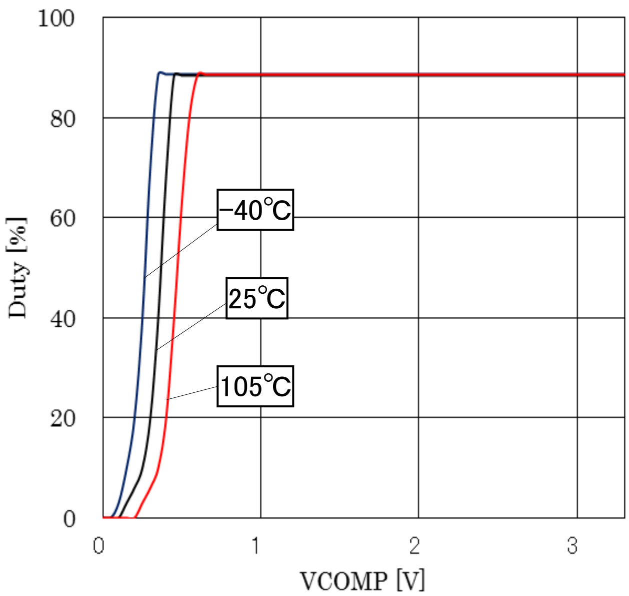


Figure 11. COMP V.S.DUTY

●**Electrical characteristic curves (Reference data)**
(Unless otherwise specified VIN = 3.3V, AVDD = 10V and Ta=25℃)

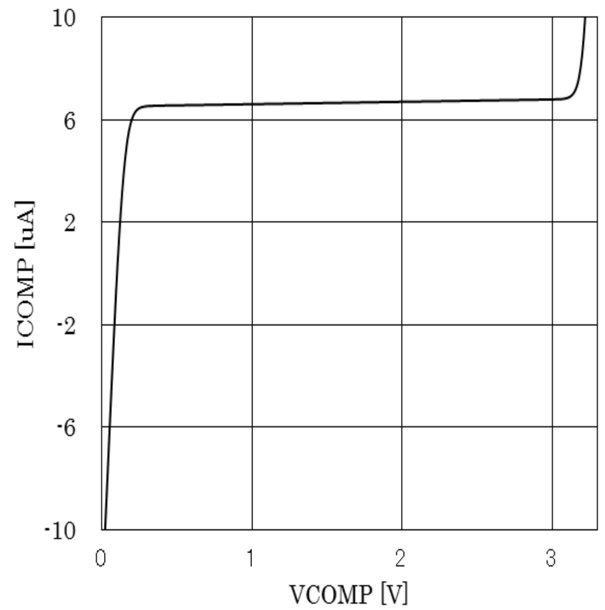


Figure 12. COMP Sink Current

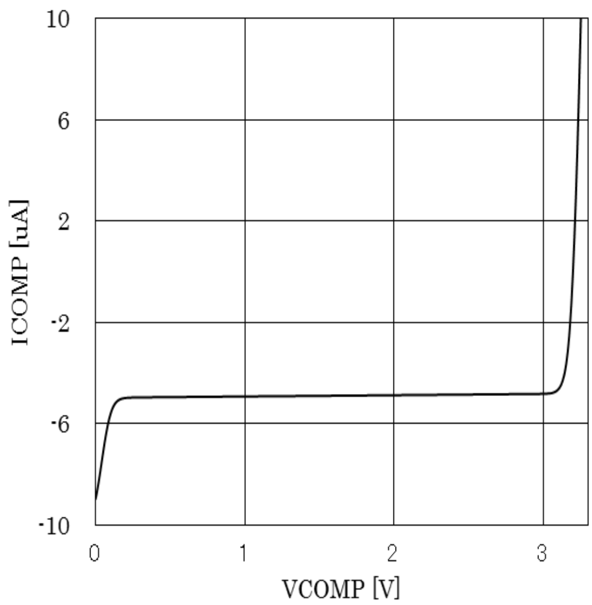


Figure 13. COMP Source Current

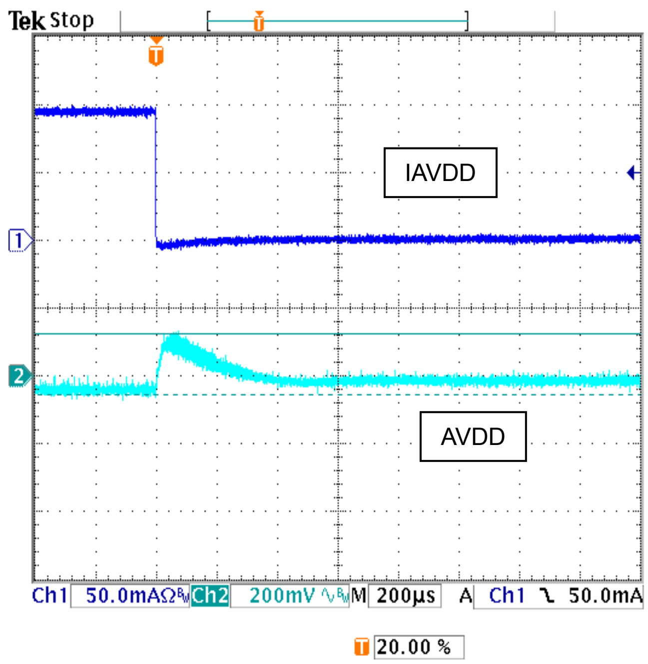


Figure 14. Load Transient Response Falling

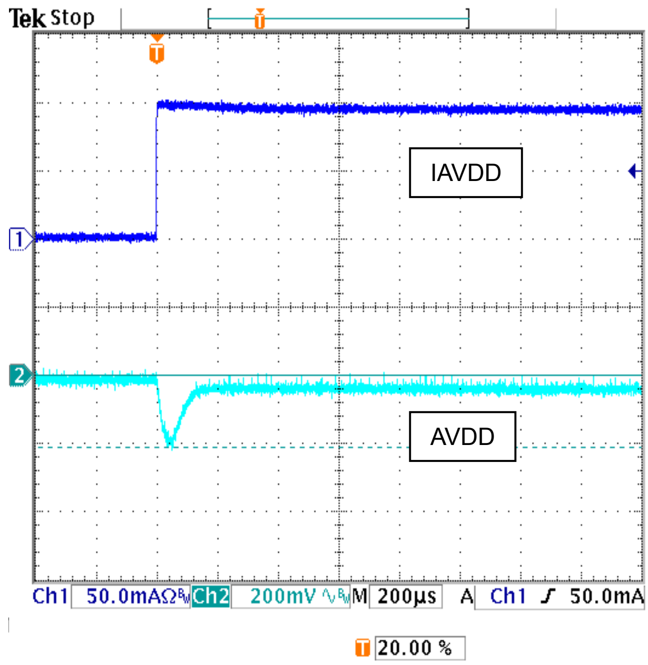


Figure 15. Load Transient Response Rising

●**Electrical characteristic curves (Reference data) – Continued**

(Unless otherwise specified VIN = 3.3V, AVDD = 10V and Ta=25℃)

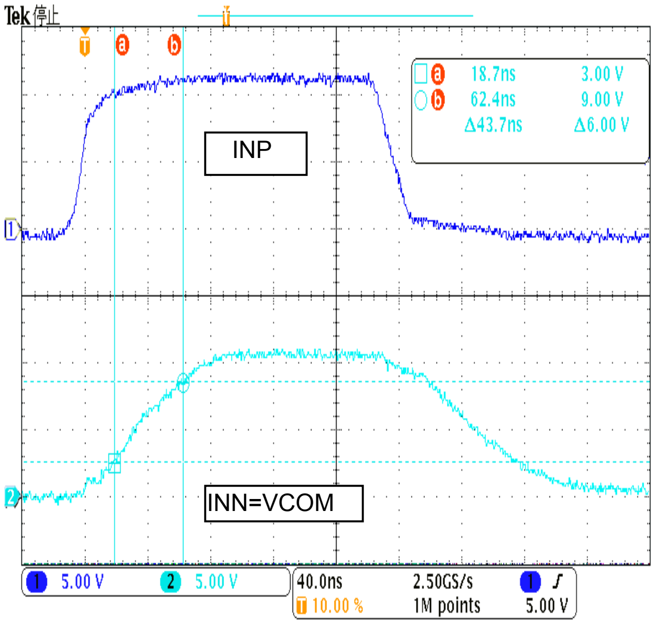


Figure 16. VCOM Slew Rate (Rising)

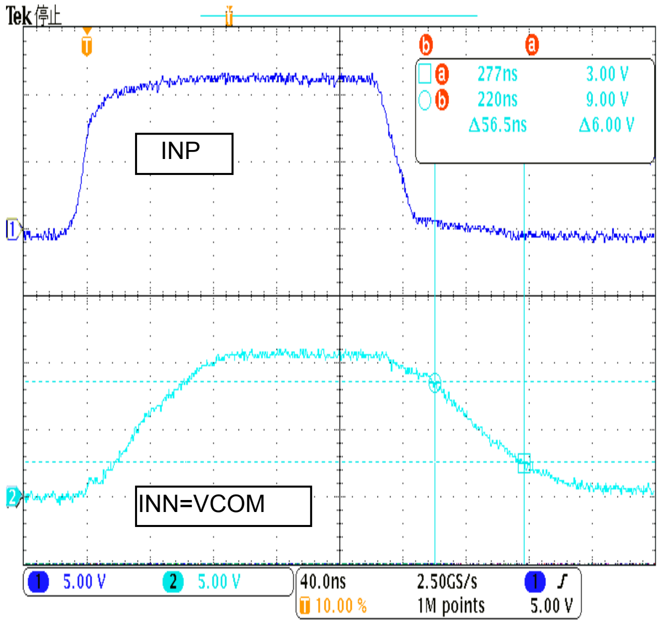


Figure 17. VCOM Slew Rate (falling)

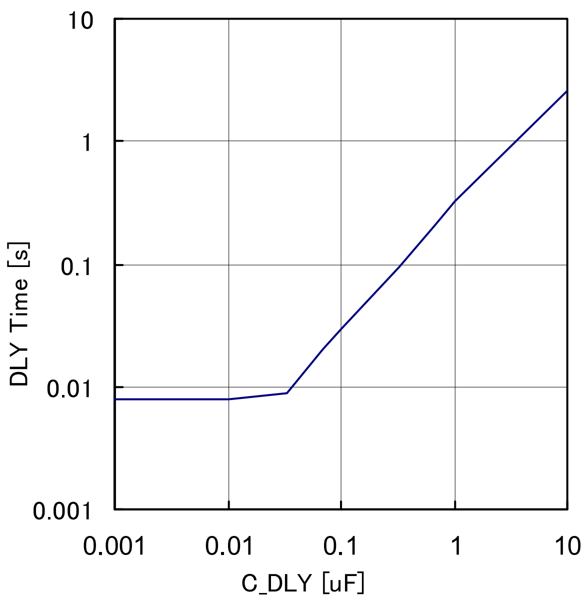


Figure 18. C_DLY vs. delay time

● **Electrical characteristic curves (Reference data) – Continued**

(Unless otherwise specified VIN = 3.3V, AVDD = 10V and Ta=25℃)

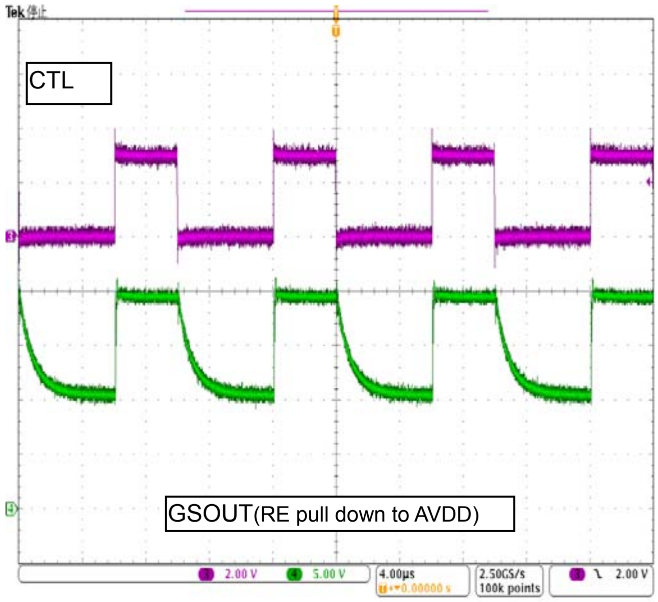


Figure 19. Gate Shading Wave form1

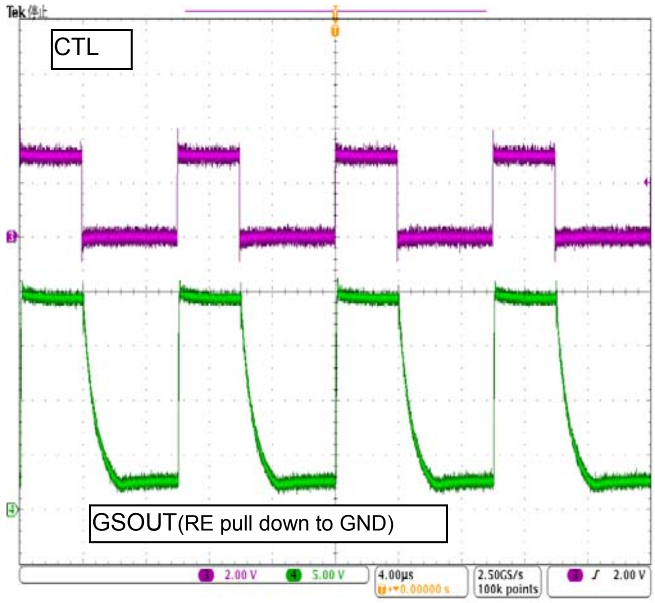


Figure 20. Gate Shading Wave form2

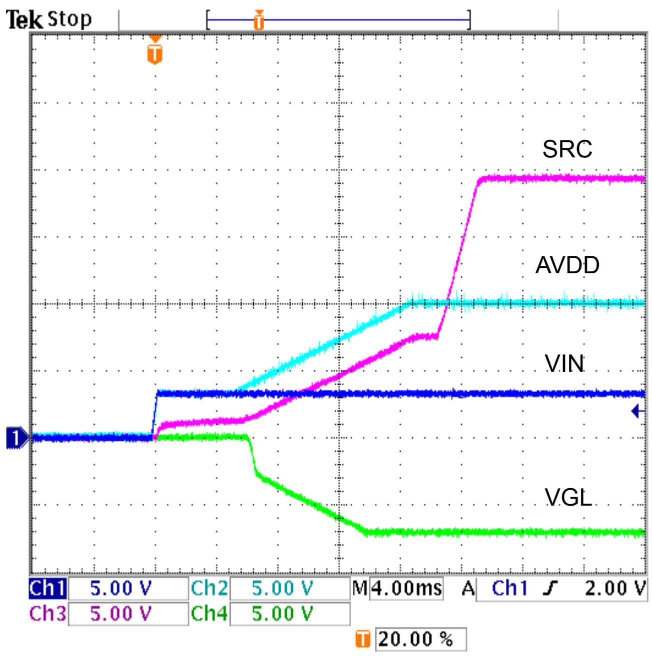


Figure 21. Power On Sequence1
(Main Output)

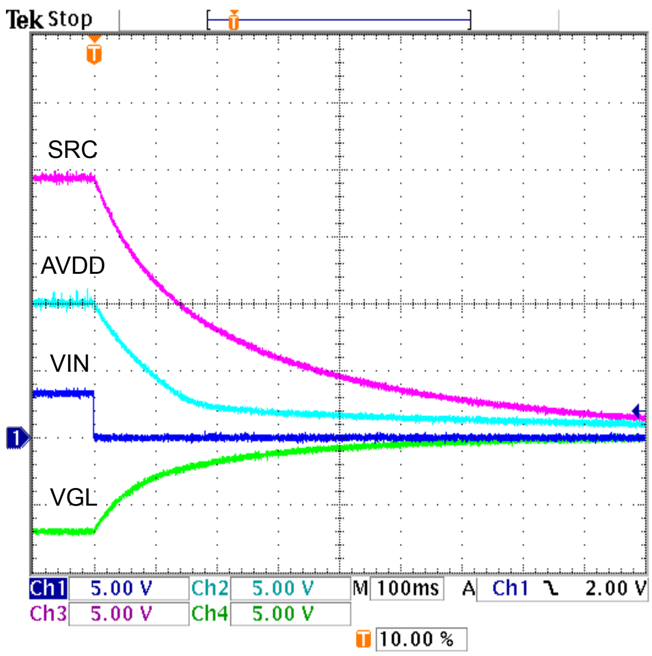


Figure 22. Power Off Sequence1
(Main Output)

●**Electrical characteristic curves (Reference data) – Continued**

(Unless otherwise specified VIN = 3.3V, AVDD = 10V and Ta=25℃)

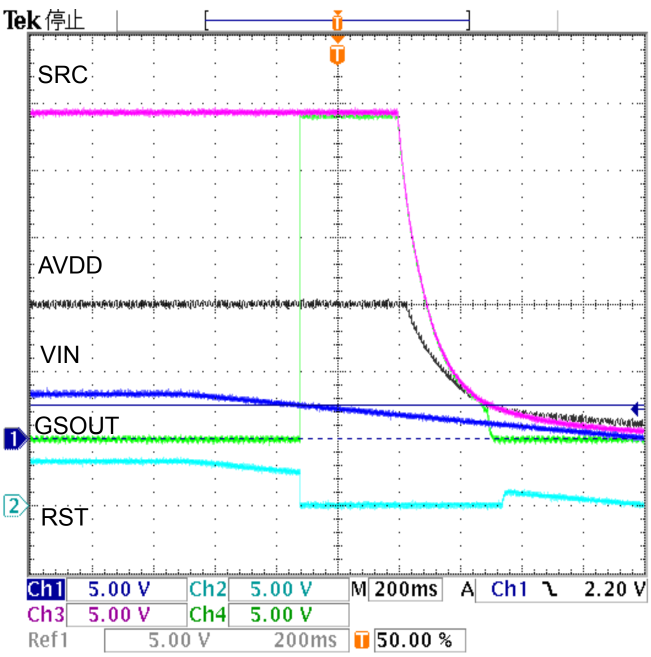


Figure 23. Power Off Sequence2
(R_RST_U=10k,R_RST_D=10k)

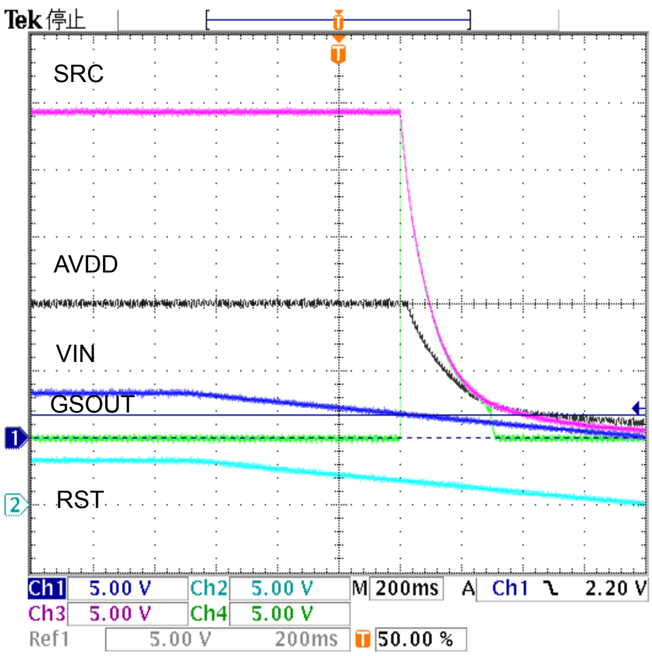


Figure 24. Power Off Sequence3
(R_RST_U=10k,R_RST_D=OPEN)

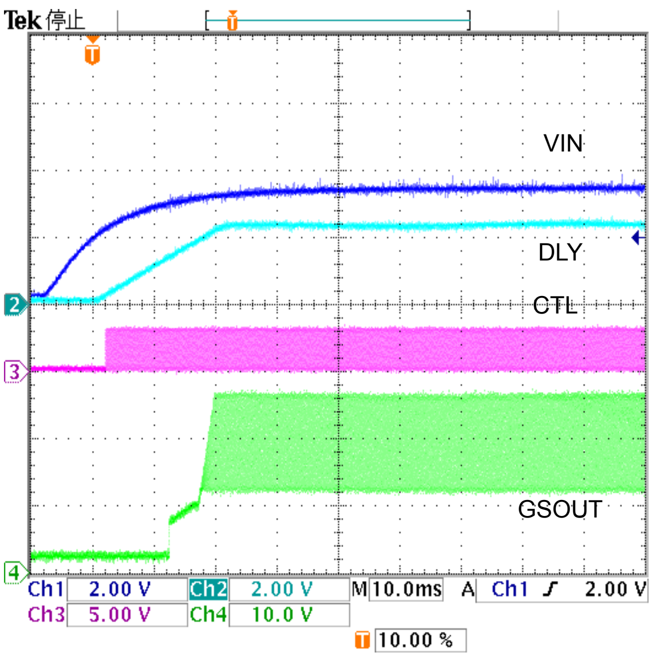


Figure 25. Power On Sequence2
(CTL=signal, RE pull down to AVDD)

●Application Example

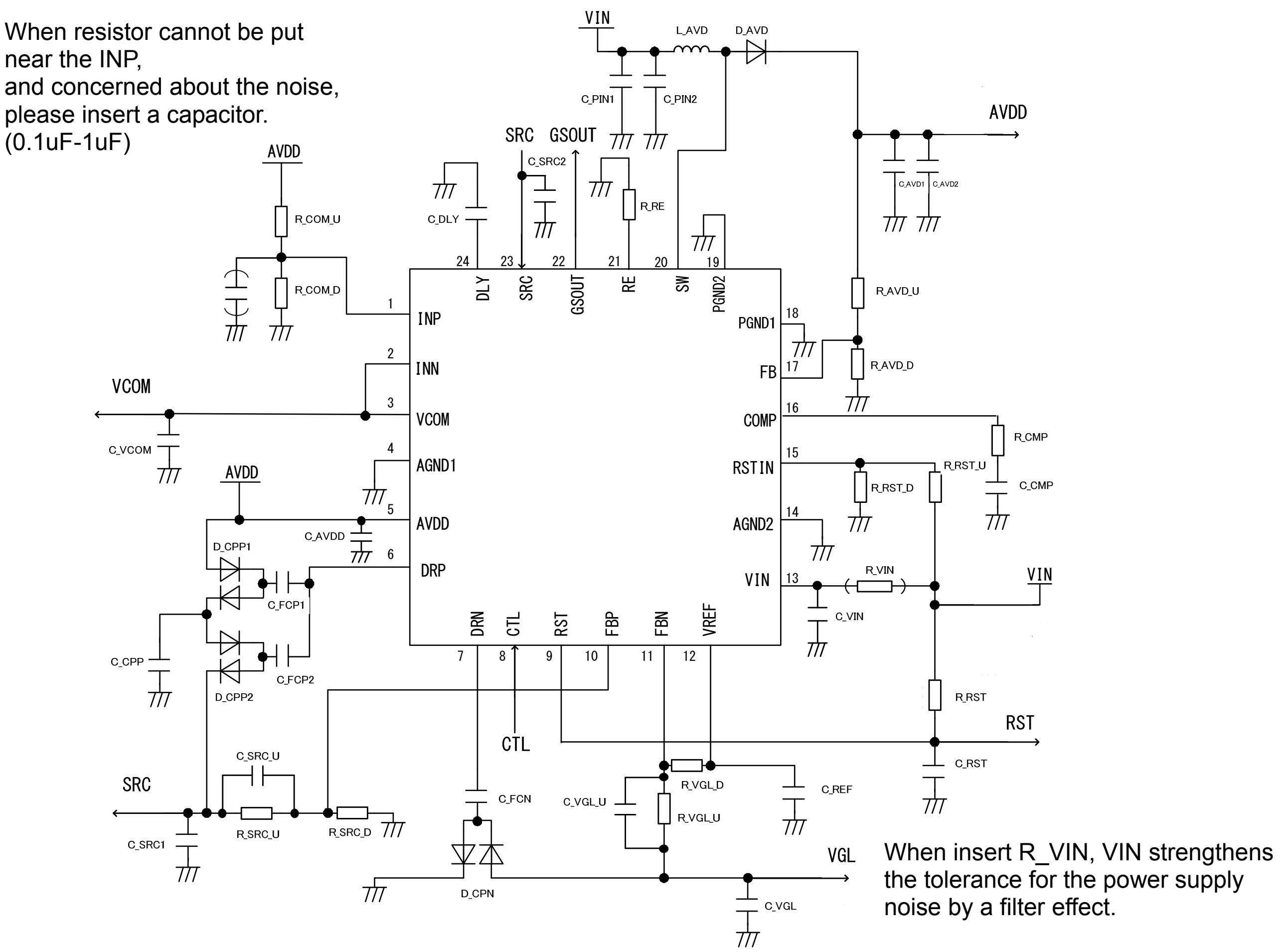


Figure 26. Application Example

Application circuit components list (VIN=3.3V, AVDD=10V, SRC=20V, VGL=-7.1V, VCOM=5V)

Parts name	Value			Unit	Company	Parts Number
	Min	Typ	Max			
C_VIN	0.47	1.0	-	uF	TDK	CGA3E1X7R1C105M
R_VIN	1	10	20	Ω	ROHM	MCR03
C_PIN1	4.7	10	-	uF	TDK	CGA5L1X7R1C106M
C_PIN2	4.7	10	-	uF	TDK	CGA5L1X7R1C106M
C_AVD1	4.7	10	22	uF	TDK	CGA5L1X7R1E106M
C_AVD2	4.7	10	22	uF	TDK	CGA5L1X7R1E106M
L_AVD	4.7	10	22	uH	TDK	LTF5022T-100M1R3-H
D_AVD	-	30/5	-	V/A	ROHM	RB080L-30DD
R_AVD_U	6.8	91	330	kΩ	ROHM	MCR03
R_AVD_D	6.8	13	330	kΩ	ROHM	MCR03
R_CMP	-	24	-	kΩ	ROHM	MCR03
C_CMP	-	2200	-	pF	TDK	CGA3E2X7R1H222M
R_RST_U	-	10	-	kΩ	ROHM	MCR03
R_RST_D	-	10	-	kΩ	ROHM	MCR03
R_RST	-	10	-	kΩ	ROHM	MCR03
C_RST	-	1.0	-	uF	TDK	CGA3E1X7R1C105M
C_DLY	10	33	100	nF	TDK	CGA3E2X7R1H333M
R_RE	0.2	1.0	5.1	kΩ	ROHM	MCR03
C_AVDD	0.047	0.1	-	uF	TDK	CGA3E2X7R1H104M
C_REF	0.1	0.22	0.47	uF	TDK	CGA3E2X7R1C224M

Parts name	Value			Unit	Company	Parts Number
	Min	Typ	Max			
C_VGL	0.47	1.0	10	uF	TDK	CGA3E1X7R1C105M
C_FCN	0.047	0.1	1.0	uF	TDK	CGA3E2X7R1H104M
D_CPN	-	80/100	-	V/mA	ROHM	DAN217UMFH
R_VGL_U	6.8	120	330	kΩ	ROHM	MCR03
R_VGL_D	6.8	16	330	kΩ	ROHM	MCR03
C_VGL_U	10	100	4700	pF	TDK	CGA3E2NP01H101J
C_SRC1	0.47	1.0	10	uF	TDK	CGA4J3X7R1H105M
C_FCP1	0.047	0.1	1.0	uF	TDK	CGA3E2X7R1H104M
C_FCP2	0.047	0.1	1.0	uF	TDK	CGA3E2X7R1H104M
C_CPP	0.047	0.1	1.0	uF	TDK	CGA3E2X7R1H104M
D_CPP1	-	80/100	-	V/mA	ROHM	DAN217UMFH
D_CPP2	-	80/100	-	V/mA	ROHM	DAN217UMFH
R_SRC_U	6.8	150	330	kΩ	ROHM	MCR03
R_SRC_D	6.8	10	330	kΩ	ROHM	MCR03
C_SRC_U	10	100	4700	pF	TDK	CGA3E2NP01H101J
C_SRC2	0.47	1.0	10	uF	TDK	CGA4J3X7R1H105M
R_COM_U	6.8	51	330	kΩ	ROHM	MCR03
R_COM_D	6.8	51	330	kΩ	ROHM	MCR03
C_VCOM	0.1	1.0	10	uF	TDK	CGA3E1X7R1E105M

※Please set in consideration of temperature properties and DC bias properties not to become less than the minimum.
COMP parts and the coil need adjustment by output voltage and load. Please consider it based on enough evaluations with the actual model.

●**Power Sequence**

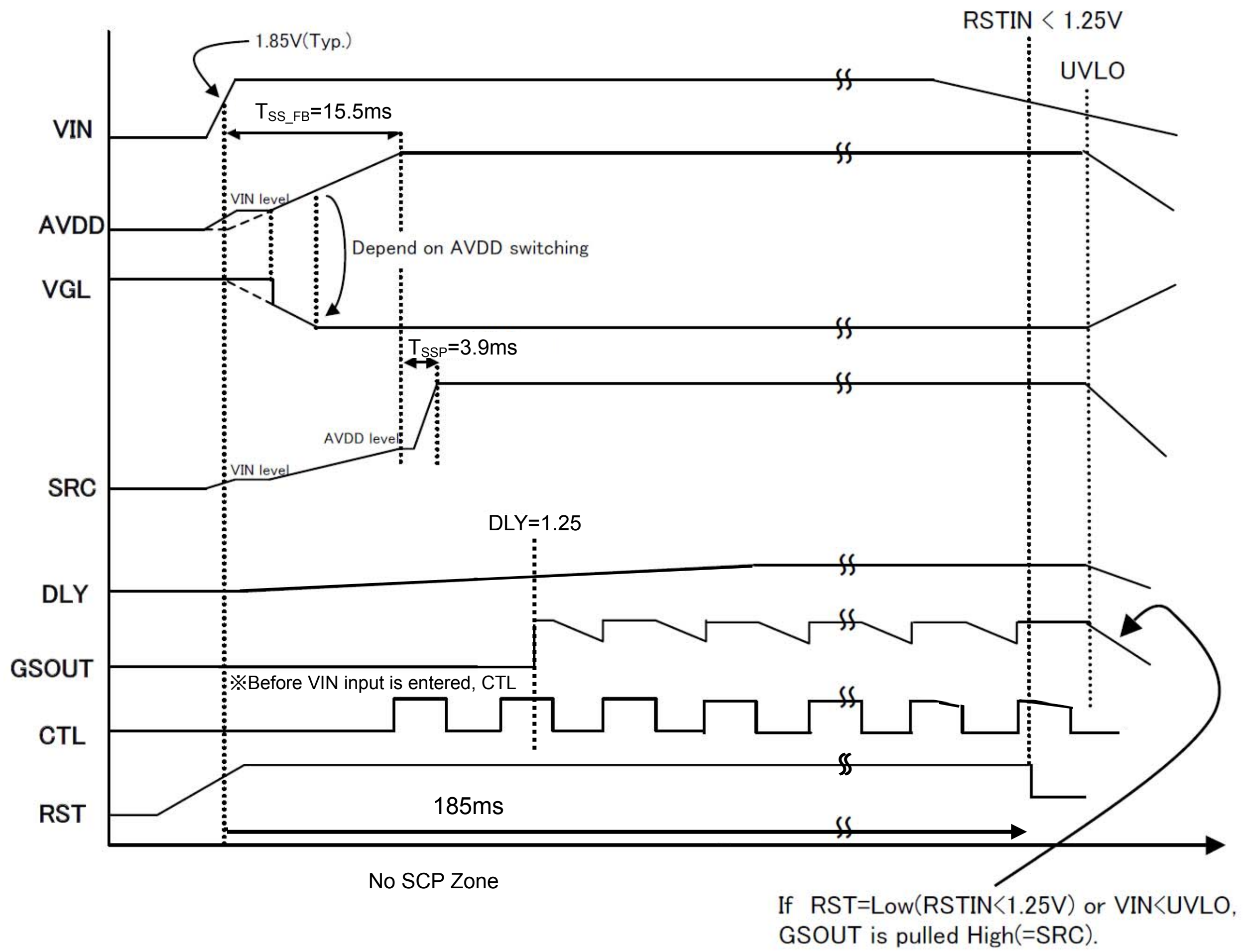


Figure 27. Power Sequence

●**Protect Operation**

・VIN UVLO

	AVDD	SRC	VGL
Falling (Typ.)	1.65V		
Rising (Typ.)	1.85V		
Action	All channels shut-down. Start-up Sequence Resets.		

・Thermal Shutdown

	AVDD	SRC	VGL
Threshold (Typ.)	160℃		
Action	All channels are latched in shut-down condition as soon as detecting Thermal Shutdown. For Recovery, power supply should be inputted under UVLO voltage.		

・Over Voltage Protection

	AVDD
Threshold (Typ.)	20V
Action	STOP switching of AVDD.

・Under Voltage Protect

	AVDD
Threshold (Typ.)	1.3V
Action	STOP switching of AVDD.

・Over Current Protect

	AVDD
Threshold (Min.)	2.5A
Action	STOP switching of AVDD.

・Short Circuit Protect

	AVDD	SRC	VGL
Threshold (Typ.)	AVDD x 0.8	SRC x 0.8	VGL x 0.8
Action	All channels are latched in shut-down condition after 63msec(Typ.) detecting Short Circuit Protect in any channel. For Recovery, power supply should be inputted under UVLO voltage.		

●**Reset Function**

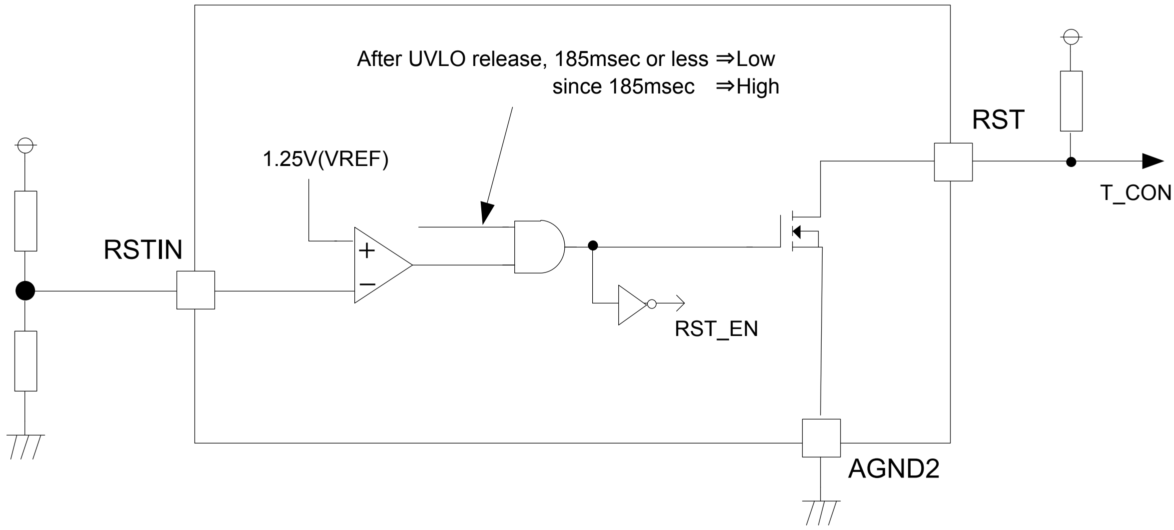


Fig.28 Reset Explanation

The RST is set to Low when the RSTIN voltage is less than 1.25V and is set to High (pulled-up by a resistor to VIN) when the RSTIN voltage is greater than or equal to 1.25V. However, during the time when power supply is ON for 185ms (Typ), RST is held High regardless of RSTIN voltage.
Gate Shading function is activated when RST_EN is High. When RSTIN is Low, the Gate Shading function cannot be used. If the Gate Shading function will not be used, the SRC, RE, and CTL must be pulled-down by a resistor or connected to GND.

●Gate Shading Function

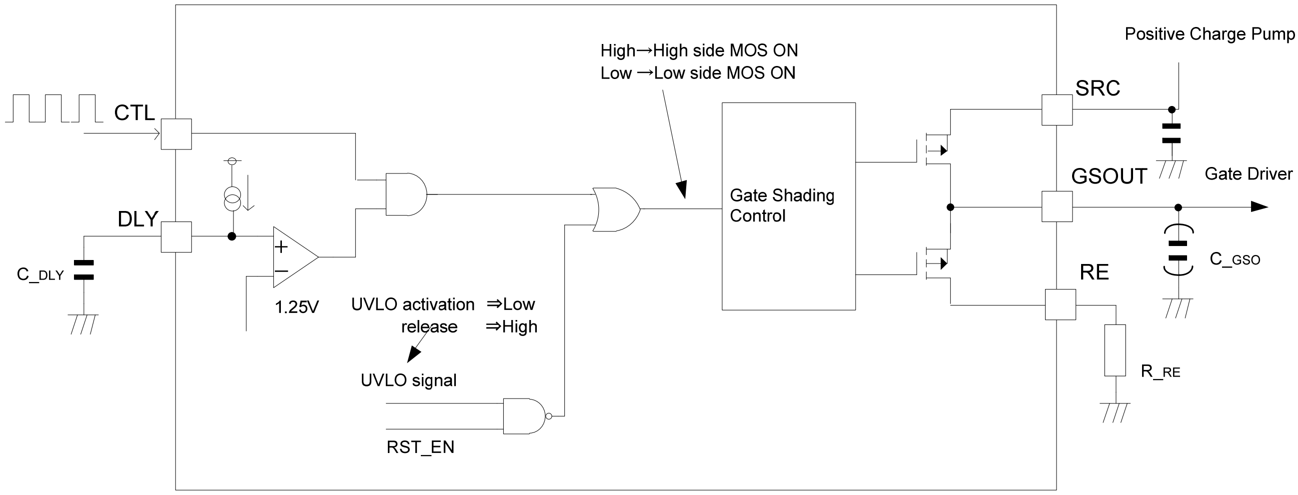


Fig.29 Gate Shading Explanation

To control the Gate Shading output (GSOUT) by the CTL input, the RSTIN and DLY pin voltages must be set greater than 1.25V. If the DLY pin is left open, the DLY voltage immediately becomes High (greater than 1.25V) when the power supply is turned ON. To add a delay time (t_DELAY) before DLY voltage becomes High, connect a capacitor (C_{DLY}) to the DLY pin The delay time (t_DELAY) can be calculated using the following formula.

$$t\_DELAY = (C\_{DLY} \times 1.25V)/5uA \qquad [sec]$$

When the CTL input is High (0.65×VIN to VIN), the MOS between SRC and GSOUT turns ON and sets the output voltage of GSOUT equal to SRC.
When the CTL input is Low (0 to 0.25×VIN), the MOS between GSOUT and RE turns ON, and GSOUT will be discharged down to RE voltage by a slope decided by the external resistor (R_RE) and capacitor (C_GSO).
To adjust a slope, the following setting value is recommended; for resistor (R_RE):200 Ω - 5.1kΩ, for capacitor (C_GSO):less than 0.1uF. It may cause the efficiency aggravation by setting out of this range.
The voltage ΔV that GSOUT discharges during the time (t_WL) when CTL input is Low can be calculated using the following formula.

$$\Delta V = SRC \times \left(1 - \exp\left(-\frac{t\_{WL}}{C\_{GSO} \times R\_{RE}}\right)\right) \qquad [V]$$

But the loss occurs when C_GSO is added. The loss ΔP can be calculated using the following formula.

$$\Delta P = Frequency(CTL) \times \Delta V^2 \times C\_{GSO} \qquad [V]$$

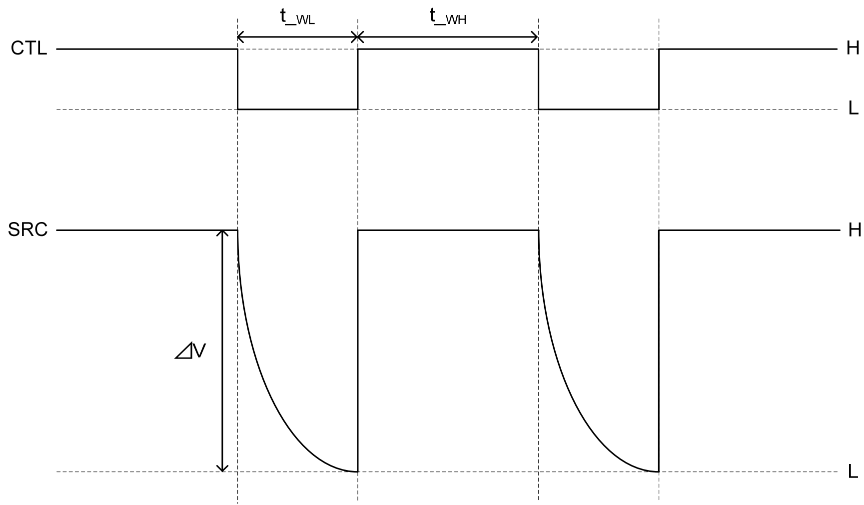


Fig.30 Gate Shading I/O Waveform

If the Gate Shading function will not be used, the SRC, RE, and CTL must be pulled-down by a resistor or connected to GND. And the DLY, please connect capacitor because there is the concern such as noises.

●How to select parts of application

(1-1) Setting the Output L Constant (Boost Converter)

The coil to use for output is decided by the rating current I_{LR} and input current maximum value I_{INMAX} of the coil.

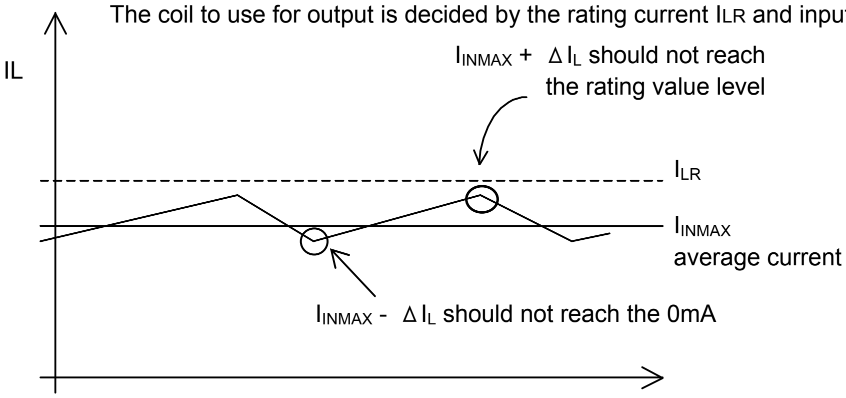


Figure 31. Coil Current Waveform

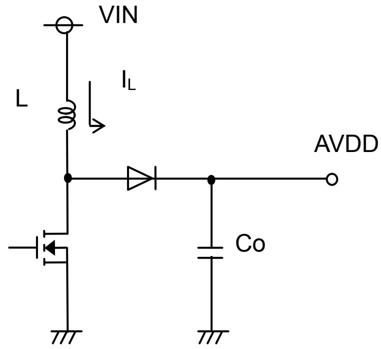


Figure 32. Output Application Circuit Diagram

Adjust so that $I_{INMAX} + \Delta I_L$ does not reach the rating current value I_{LR}. In addition, become the Discontinuous Condition Mode (DCM) when IL reaches 0mA. As for the section which DCM and Continuous Condition Mode (CCM) are replaced by, jitter properties turn worse. Adjust the coil so that $I_{INMAX} - \Delta I_L$ does not reach the 0mA. ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \; VIN \times \frac{AVDD - VIN}{AVDD} \times \frac{1}{f} \quad [A]$$

Here, f is the switching frequency.

Set with sufficient margin because the coil value may have the dispersion of ±30%. If the coil current exceeds the rating current I_{LR} of the coil, it may damage the IC internal element.

BD81842MUV-M uses the current mode DC/DC converter control and has the optimized design at the coil value. A coil inductance (L) of 4.7 uH to 22 uH is recommended from viewpoints of electric power efficiency, response, and stability.

(2) Output Capacity Settings

For the capacitor to use for the output, select the capacitor which has the larger value in the ripple voltage V_{PP} allowance value and the drop voltage allowance value at the time of sudden load change. Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = I_{LMAX} \times R_{ESR} + \frac{1}{fCo} \times \frac{VIN}{AVDD} \times \left(I_{LMAX} - \frac{\Delta I_L}{2}\right) \quad [V]$$

Here, f is the switching frequency and RESR is ESR of output capacitor.

Perform setting so that the voltage is within the allowable ripple voltage range.

For the drop voltage during sudden load change; V_{DR}, please perform the rough calculation by the following equation.

$$V_{DR} = \frac{\Delta I}{Co} \times 10\ us \quad [V]$$

However, 10 μs is the rough calculation value of the DC/DC response speed. Please set the capacitance considering the sufficient margin so that these two values are within the standard value range.

(3) Selecting the Input Capacitor

Since the peak current flows between the input and output at the DC/DC converter, a capacitor is required to install at the input side. For the reason, the low ESR capacitor is recommended as an input capacitor which has the value more than 10 μF and less than 100 mΩ. If a capacitor out of this range is selected, the excessive ripple voltage is superposed on the input voltage, accordingly it may cause the malfunction of IC.

However these conditions may vary according to the load current, input voltage, output voltage, inductance and switching frequency. Be sure to perform the margin check using the actual product.

(4) Setting R_C, C_C of the Phase Compensation Circuit

In the current mode control, since the coil current is controlled, a pole (phase lag) made by the CR filter composed of the output capacitor and load resistor will be created in the low frequency range, and a zero (phase lead) by the output capacitor and ESR of capacitor will be created in the high frequency range. In this case, to cancel the pole of the power amplifier, it is easy to compensate by adding the zero point with C_C and R_C to the output from the error amp as shown in the illustration.

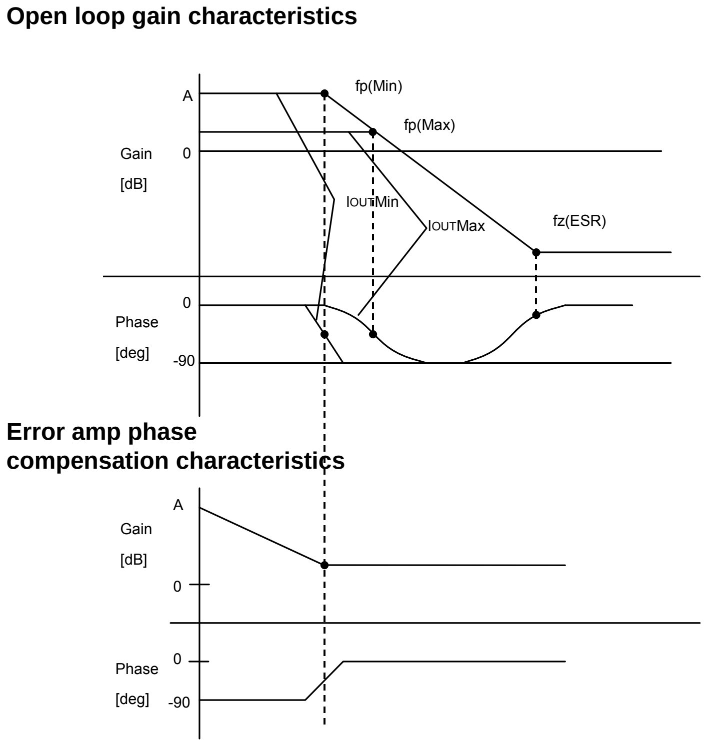


Figure 33. Gain vs Phase

$$Fp = \frac{1}{2\pi \times R_O \times C_O} \text{ [Hz]}$$

$$fz(ESR) = \frac{1}{2\pi \times E_{SR} \times C_O} \text{ [Hz]}$$

Pole at the power amplification stage

When the output current reduces, the load resistance R_o increases and the pole frequency lowers.

$$fp(Min) = \frac{1}{2\pi \times R_{OMax} \times C_O} \text{ [Hz]} \leftarrow \text{at light load}$$

$$fz(Max) = \frac{1}{2\pi \times R_{OMin} \times C_O} \text{ [Hz]} \leftarrow \text{at heavy load}$$

Zero at the power amplification stage

When the output capacitor is set larger, the pole frequency lowers but the zero frequency will not change. (This is because the capacitor ESR becomes 1/2 when the capacitor becomes 2 times.)

$$fp(Amp.) = \frac{1}{2\pi \times R_c \times C_c} \text{ [Hz]}$$

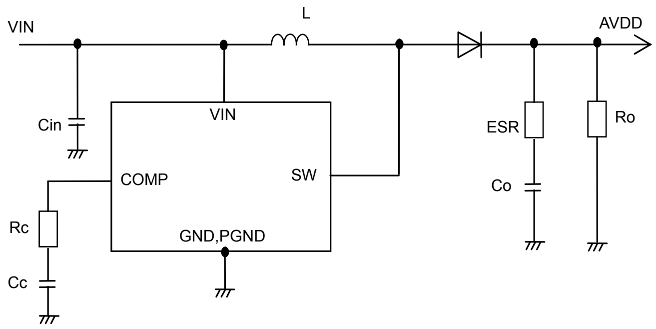


Figure 34. Application Circuit Diagram

It is possible to realize the stable feedback loop by canceling the pole fp(Min.), which is created by the output capacitor and load resistor, with CR zero compensation of the error amp as shown below.

fz(Amp.) = fp(Min.)

$$\longrightarrow \frac{1}{2\pi \times Rc \times Cc} = \frac{1}{2\pi \times Romax \times Co} \text{ [Hz]}$$

(5) Design of the Feedback Resistor Constant

Refer to the following equation to set the feedback resistor. As the setting range, 6.8 kΩ to 330 kΩ is recommended. If the resistor is set lower than a 6.8 kΩ, it causes the reduction of power efficiency. If it is set more than 330 kΩ, the offset voltage becomes larger by the input bias current 0.1 μA(Typ.) in the internal error amplifier.

$$AVDD = \frac{R\_AVD\_U + R\_AVD\_D}{R\_AVD\_D} \times FB \quad [V]$$

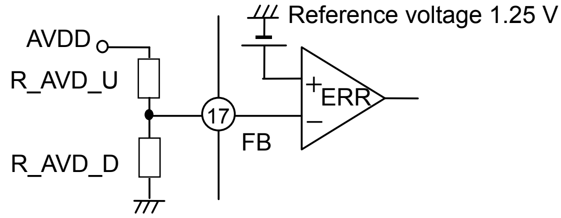


Figure 35. Application Circuit Diagram

(6) Positive-side Charge Pump Settings

The IC incorporates a charge pump controller, thus making it possible to generate stable gate voltage.
The output voltage is determined by the following formula. As the setting range, 6.8 kΩ to 330 kΩ is recommended.
If the resistor is set lower than a 6.8kΩ, it causes the reduction of power efficiency. If it is set more than 330 kΩ, the offset voltage becomes larger by the input bias current 0.1 μA (Typ.) in the internal error amp.

$$SRC = \frac{R\_SRC\_U + R\_SRC\_D}{R\_SRC\_D} \times FBP \quad [V]$$

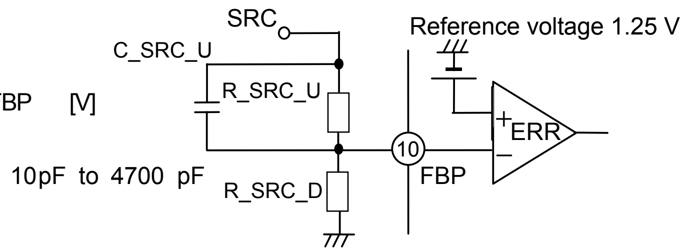


Figure 36. Application Circuit Diagram

In order to prevent output voltage overshooting, add capacitor C_SRC_U in parallel with R_SRC_U. The recommended capacitance is 10 pF to 4700 pF. But please enough evaluate with the actual model because adjustments in the application may be necessary.

Please meet the following condition about the number of the steps of the charge pump. In addition, confirm with an actual model for the last time. Because the loss is increase when a calculation result is the small, please be careful.

$$\frac{SRC}{(n+1) \times AVDD - 2n \times Vf} < 1$$

Here, n is the steps of charge pump, Vf is the forward voltage of diode.

(7) Negative-side Charge Pump Settings

This IC incorporates a charge pump controller for negative voltage, thus making it possible to generate stable gate voltage.

The output voltage is determined by the following formula. As the setting range, 6.8 kΩ to 330 kΩ is recommended. If the resistor is set lower than a 6.8 kΩ, it causes the reduction of power efficiency. If it is set more than 330 kΩ, the offset voltage becomes larger by the input bias current 0.1 µA (Typ.) in the internal error amp.

$$V_{GL} = (FBN - VREF)\frac{R\_VGL\_U}{R\_VGL\_D} + FBN \quad [V]$$

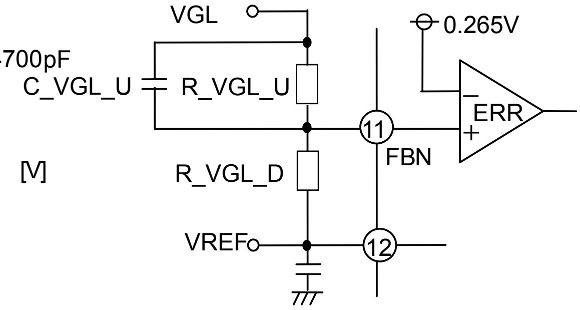


Figure 37. Application Circuit Diagram

In order to prevent output voltage overshooting, insert capacitor C_VGL_U in parallel with R_VGL_U. The recommended capacitance is 10 pF to 4700 pF. But please enough evaluate with the actual model because adjustments in the application may be necessary.

Please meet the following condition about the number of the steps of the charge pump. In addition, confirm with an actual model for the last time. Because the loss is increase when a calculation result is the small, please be careful.

$$\frac{-VGL}{-(n \times AVDD - 2n \times Vf)} < 1$$

Here, n is the steps of charge pump, Vf is the forward voltage of diode.

(8) VCOM Amplifier block

VCOM Amplifier is a rail-to-rail high slew rate Operational Amplifier which has 0V - AVDD voltage (the 1pin (INP) input voltage) as an input and output voltage range.

When add a capacitor to output, 0.1uF – 10uF is recommended for the reason of stability.

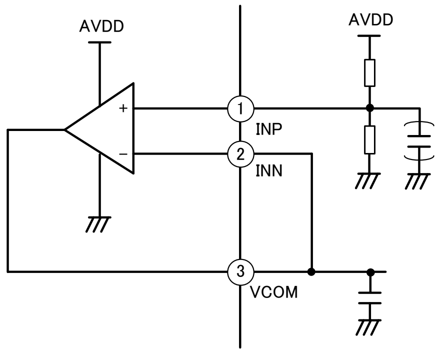


Figure 38. Application Circuit Diagram

(9) Process of unused function

When Gate Shading Function is not used, please proceed each pin (SRC, RE, CTL, DLY) as follows.

※The SRC, RE, and CTL must be pulled-down by a resistor (0Ω-10kΩ) or connected to GND. The DLY, please connect capacitor because there is the concern such as noises.

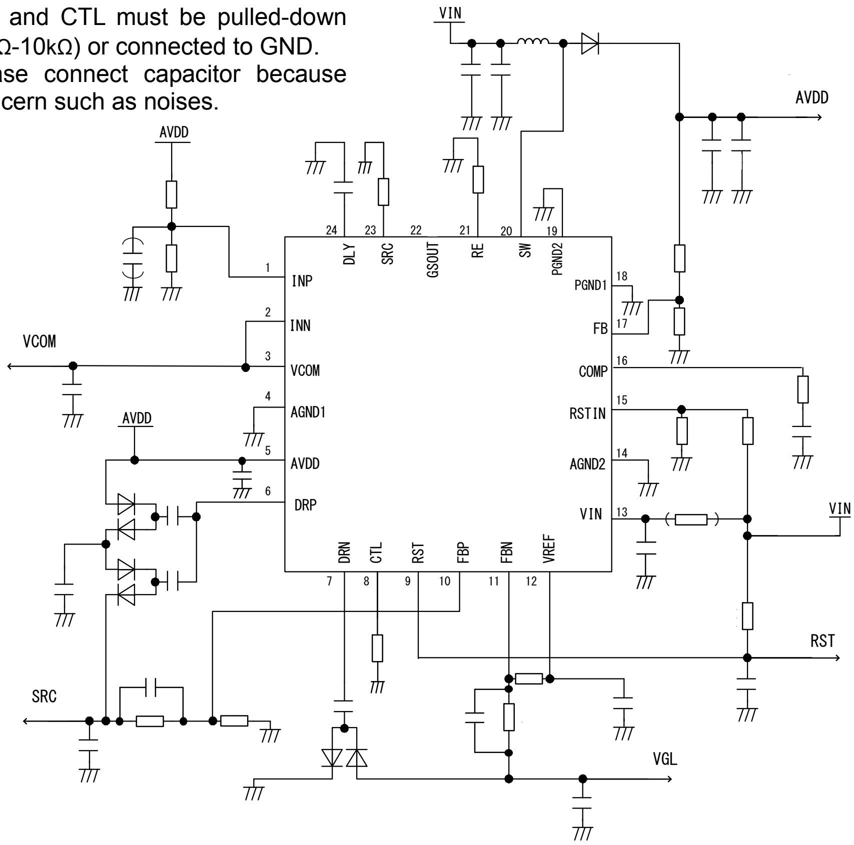


Figure 39. Application Circuit

When VCOM function is not used, please proceed each pin (INP, INN, VCOM) as follows.

※The INP must be pulled-down by a resistor (0Ω-10kΩ) or connected to GND.

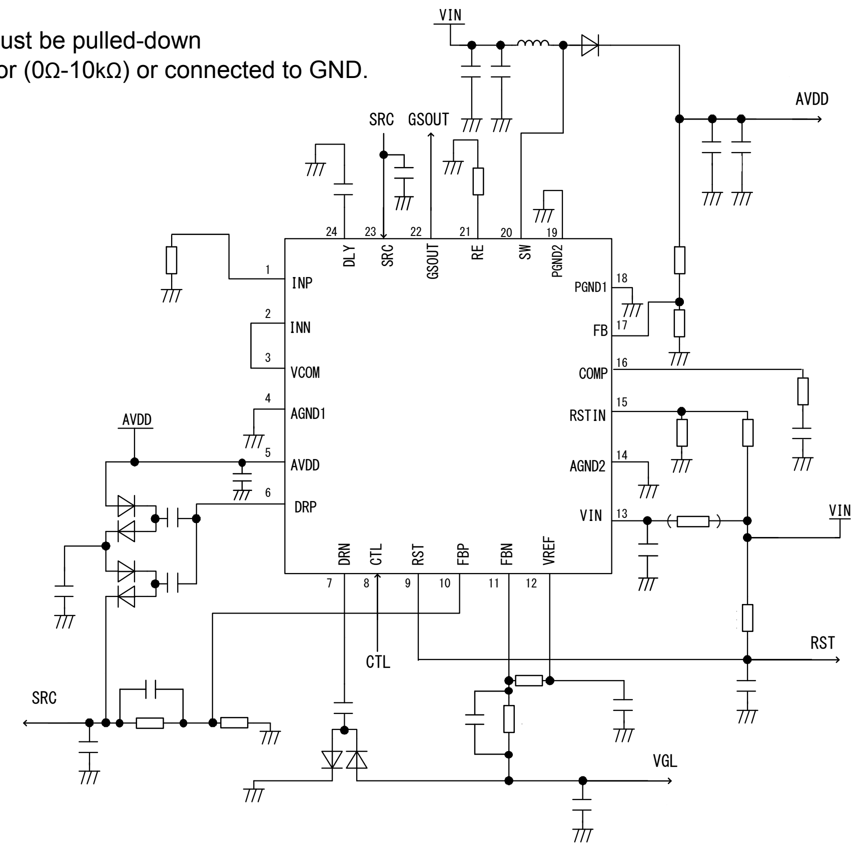


Figure 40. Application Circuit

●PCB Layout Guide

GND Wiring Pattern

The high current GND (PGND) should be wired thick. To reduce line impedance, the GND lines must be as short and thick as possible and uses few via. Therefore design at PCB board four layers or above is recommended. (Please use the middle layer as GND shielding and directly connect each GND.) In the case of two layers or less at PCB board designs, please enough confirm with the actual model about the heat and the noise with care to a GND wiring.

Switching-Line Wiring Pattern

The wiring from switching line (SW pin) of DC/DC converter to inductor and diode must be as short and thick as possible. If a wiring is long, ringing by switching increases, and the voltage over the resistance of this IC might be generated. Please note that switching line does not vary PCB layer.
Switching line and wiring easily affected by noise such as feedback line or COMP line must be placed separately. Switching noise spread may cause the lack of operation stability. In case the multi-layer PCB board, please note that a switching line and a line easily affected by noise or the external components are not adjacent between layers. Drawing GND shield line between switching line and these lines easily affected by noise is recommended if these lines are placed close.

Power Supply Voltage Line Wiring Pattern

For power supply voltage (VIN) and internal reference voltage (VREF), place smooth capacitor nearby IC pin. Especially, VIN is a power supply line of internal MOSFET for Boost DC/DC, placing capacitor at distance within 2mm from pin is needed. In addition, wire the VIN line by thickness more than 3mm.
Furthermore, insert the resistance (RC filter formation) on VIN line and become stronger in a power supply change. Please note that smooth capacitor does not vary PCB layer.

The figure 41 shows an application circuit on the basis of the basic PCB layout pattern guideline mentioned above.

- Bold line: High current line
- Blue line(two dots and dashed line): Wiring easily affected by noise
- Red line (dashed line): Noise source line such as switching line

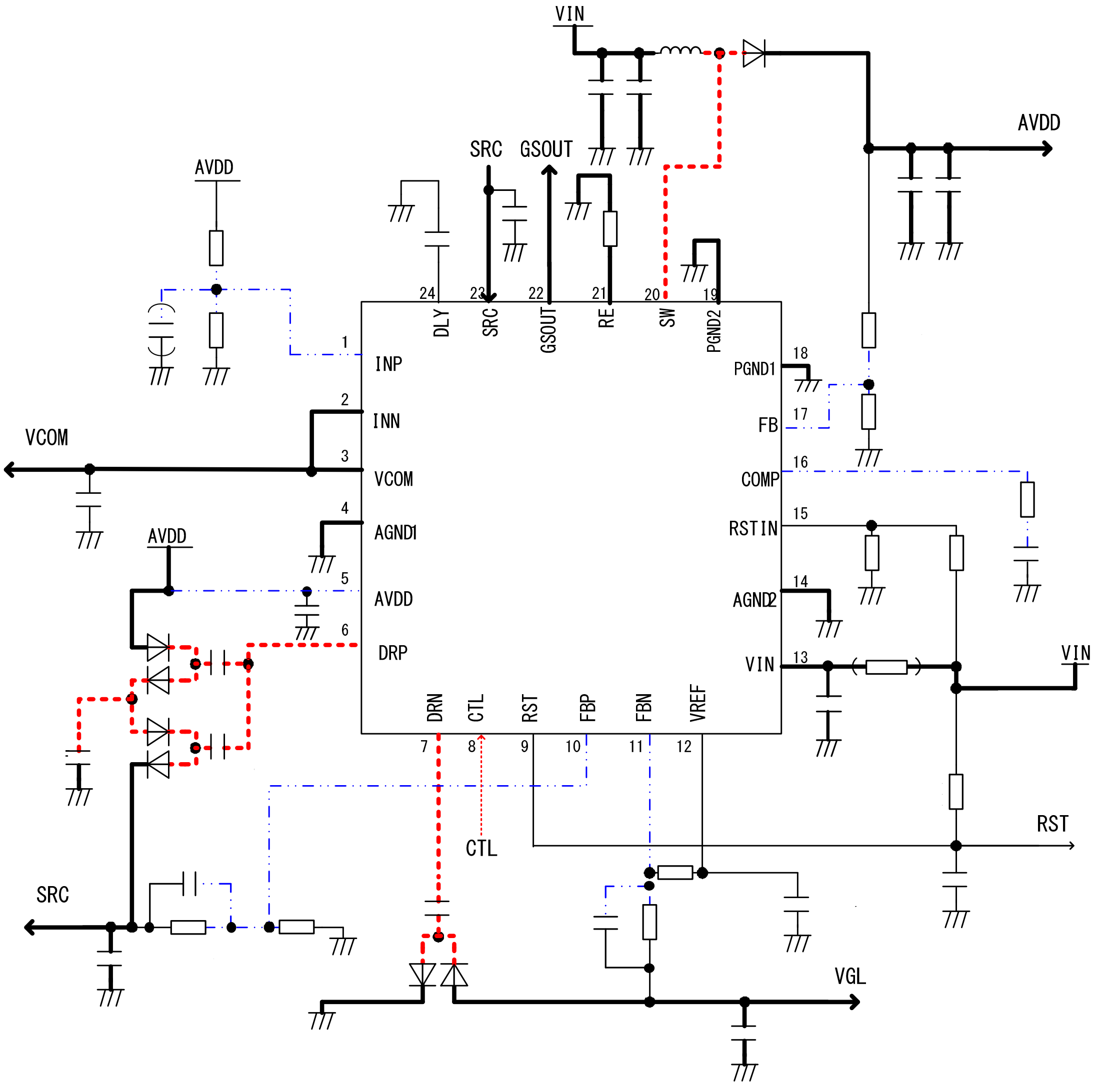


Figure 41. Application Circuit

Recommended Layout Pattern

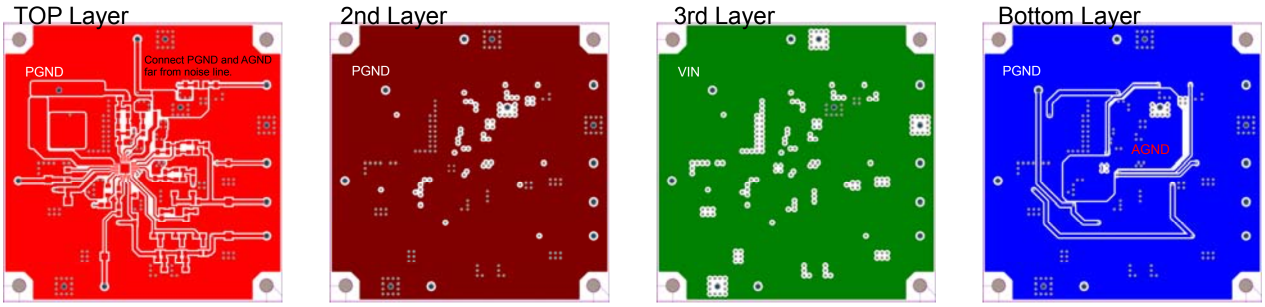


Figure 42. Recommended Layout Pattern

EMC Layout Guide

Introduce the plan that can design on the PCB as EMC measures.

Measures by the board pattern

① Wire AVDD line briefly thickly.
② Wire the current loop of Boost DC/DC briefly thickly.

Measures by the external component

③ Insert a common mode filter or a beads coil in the AVDD line and form the EMC filter.
④ Place output capacitor and small capacitor (10pF - 1,000pF) in parallel.
⑤ Insert the snubber circuit in SW pin. (Assumed the efficiency becomes worse)

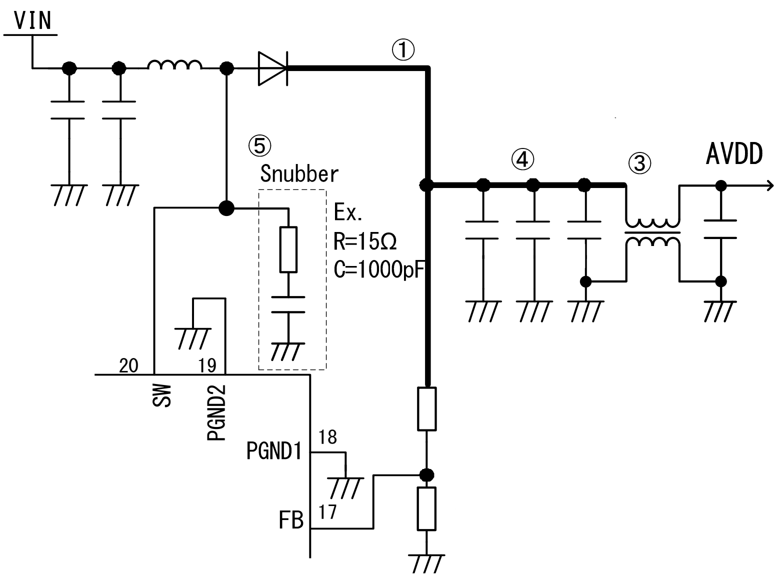


Figure 43. Application Circuit

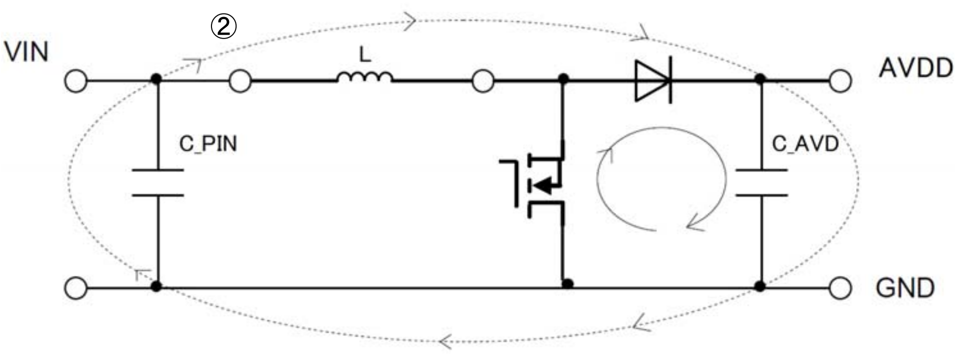
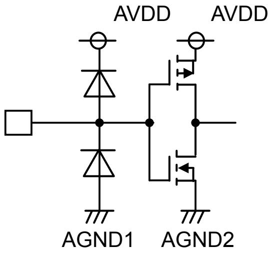
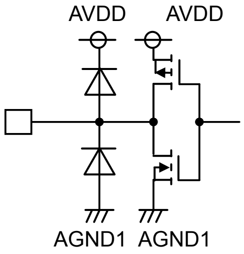
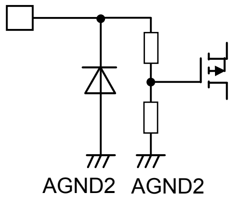
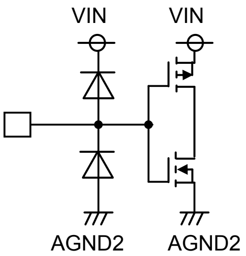
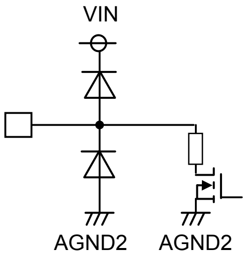
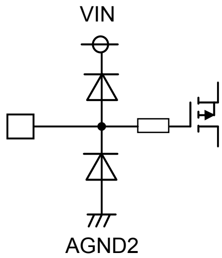
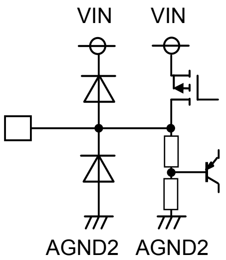
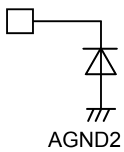
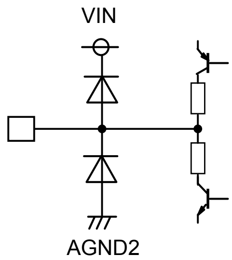
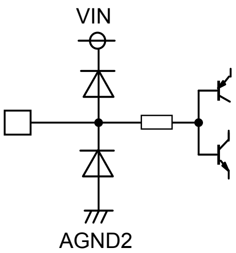
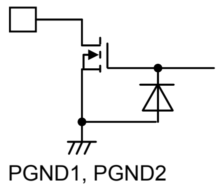
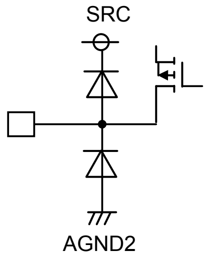
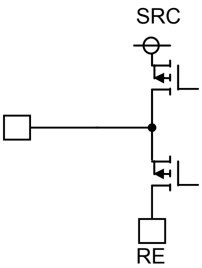
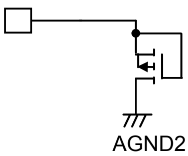
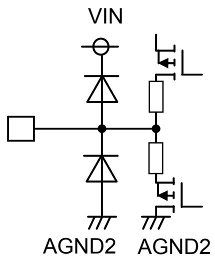


Figure 44. Current loop

●I/O Equivalent Circuit Diagrams

(Except for 4.AGND1, 14.AGND2, 18.PGND1, 19.PGND2)

1.INP 2.INN	3.VCOM 6.DRP 7.DRN	5.AVDD
		
8.CTL	9.RST	10.FBP 11.FBN 15.RSTIN
		
12.VREF	13.VIN	16.COMP
		
17.FB	20.SW	21.RE
		
22.GSOUT	23.SRC	24.DLY
		

●Operation Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

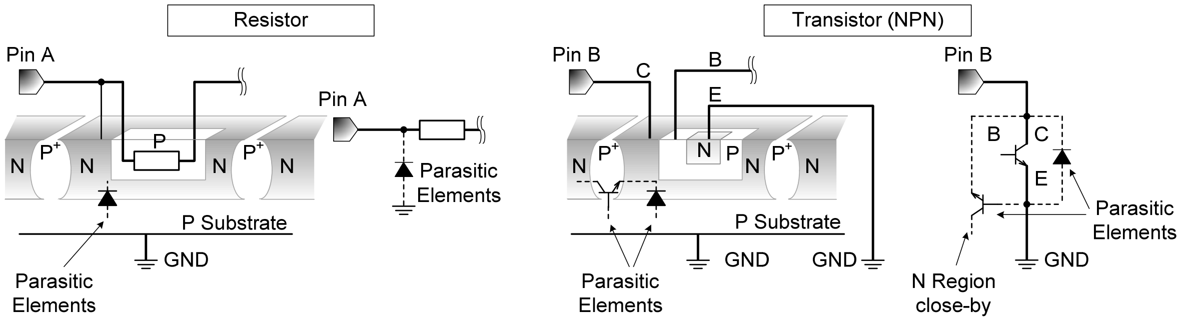


Figure 45. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

●Ordering Information

B	D	8	1	8	4	2	M	U	V	-	ME2

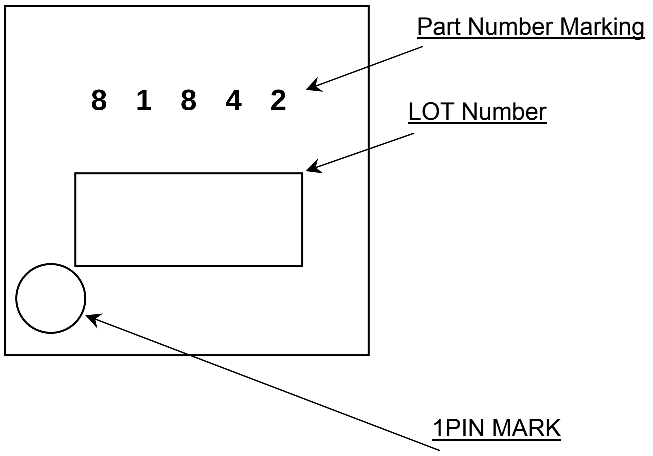
Part Number

Package
MUV:VQFN24SV4040

Product Rank
M: for Automotive
Packaging and forming specification
E2: Embossed tape and reel

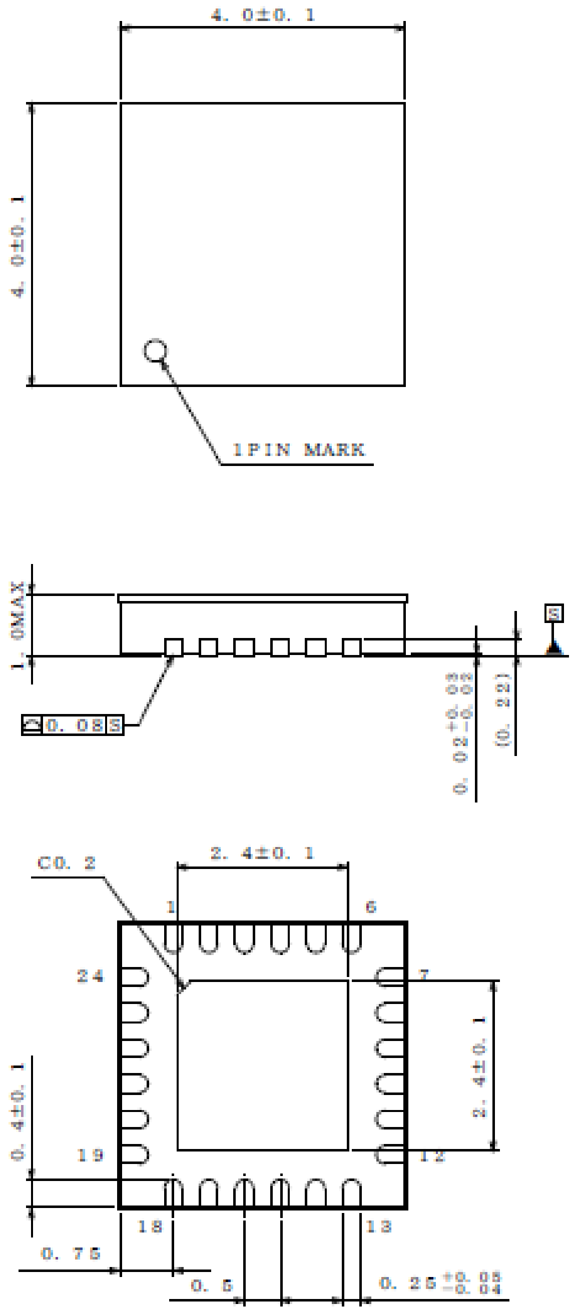
●Marking Diagrams

VQFN24SV4040 (TOP VIEW)



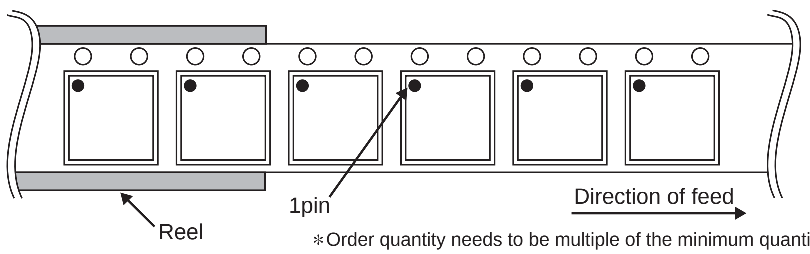
●Physical Dimension, Tape and Reel Information

Package Name	VQFN24SV4040



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Revision History

Date	Revision	Changes
07.Sep.2015	001	New Release
23.Jun.2016	002	①P6 Thermal Resistance : Footprints and Traces 74.2mm^2(Square) ⇒ 74.2mm x 74.2mm ②P25 Add Recommended Layout Pattern

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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